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MODELING AND MITIGATION OF STATIC NOISE MARGIN VARIATION IN SUB THRESHOLD SRAM CELLS

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ABSTRACT:

Static Random Access Memory (SRAM) has recently been developed into a physical unclonable function (PUF) for generating chip-unique signatures for hardware cryptography. The most compelling issue in designing a good SRAM-based PUF (SPUF) is that while maximizing the mismatches between the transistors in the cross-coupled inverters improves the quality of theSPUF, this ironically also gives rise to increased memory read/write failures. For this reason, the memory cells of existing SPUFs cannot be reused as storage elements, which increases the overheads of cryptographic system where long signatures and high-density storage are both required. In this paper, statistical models for estimating the static noise margins (SNMs) of SRAM cells are built from the perspective of a shifted voltage transfer characteristic. Read (hold) SNM of a subthreshold 8T cell is analyzed. It is shown that the distribution of a single-sided read SNM is a weighted sum of several normal distributions instead of a regular Gaussian distribution. Further, this project is enhanced by using 11T radiation tolerant memory cell. The proposed bitcell is specifically designed to enable robust, low-voltage, ULP operation in space applications and other high-radiation environments. This is achieved by employing a dual-feedback, separated-feedback mechanism to overcome the increased vulnerability due to supply voltage scaling.

KEYWORDS: Static Random Access Memory ¸Radiation tolerant, subthreshold, physical unclonable function.

INTRODUCTION:

Going with the trend of increasing connectivity and services offered by computing devices, the amount of sensitive information processed by and stored on computing devices is growin rapidly. Recently, Physical Unclonable Function (PUF) has sprouted up as a promising primitive to enforce data privacy and access control to electronic devices. Among the PUF implementations [1–5], SRAM-based PUF (SPUF) has attracted tremendous attention. This is because SRAM, being an integral part of computer memory sub-system, plays a pivotal role in trusted computing platforms. The ability to use the storage cells of SRAM inseparably as PUF will replace or augment memory curtaining as a stronger fortification to the roots of trust for memory authentication. Unfortunately, existing SPUF cells cannot be doubled as regular storage elements. The exploitation o process-variation induced device mismatches in the cross-coupled inverter cell for random, unique and reliable response bit generation is detrimental to the regular memory operation, as it will result in increased parametric failures due principally to destructive read and unsuccessful write operations Archived literatures reported wide varieties of design approaches that either improve the qualities of SPUF or harness the readability and writability of SRAM cells as data storage elements, albeit IN PORTABLE devices and implantable devices, memory operating in the subthreshold region is often used to prolong battery life. The dynamic power scales with the square of the supply voltage; the leakage power is also reduced when lowering the supply voltage. Despite the success in reducing power consumption by operating circuits in the subthreshold region, reliability becomes the most serious issue. Reduced supply voltage shrinks both the write and read (henceforth, capital letter will not be used for Read and Write operations) noise margin significantly. A more problematic issue is the serious degradation in the worst-case read stability and writability because of global and local process variations. To counteract the serious reliability degradation in low supply voltage, an 8T SRAM cell was proposed in [1] where a separate read port was employed to achieve a disturb-free read. Since then, various low-voltage SRAM cells with a dedicated read port have been proposed, including the leakage

reduced 10T cell in [2], and 9T [3] and 10T cells [4] that support a bitinterleaving array with the aim of reducing the impact of soft errors. Characterizing variation in cell stability is necessary, considering the large number of cells involved in an SRAM system. This is even more critical for SRAM systems operating in the subthreshold region because of the larger variations in static noise margin (SNM). Monte Carlo (MC) simulations are often carried out to capture the worst-case read stability. However, MC simulations for a large array are often computationally prohibitive. Importance sampling [5], [6] was proposed as a powerful technique to characterize the variation of SNM. By transforming the sampling density function, MC simulations based on importance sampling is much more efficient than traditional full MC simulations. Nevertheless, many samples are still needed. Therefore, an accurate statistical model in an analytical or a semi-analytical form is able to help designers estimate the performance of the SRAM under process variation in the early design phase without resorting to time-consuming MC simulations repeatedly.

LITERATURE SURVEY:

NVSRAM is one of the advanced NVRAM technology that is fast replacing the Battery-backed SRAMs that need battery free solutions and long term retention at SRAM speeds. For instant on-off operation better non volatile performance is essential [1].Better SRAM performance in terms of leakage power , access time ,robustness is essential [2].The average power dissipiation should be less [3].The 8T SRAM cell as compared to conventional 6T SRAM cell achieved improved read stability, read current and leakage current [4]. Write power i.e. power dissipiation in SRAM should be less [5]. The issue associated with transistor scaling and power management are addressed [8].The operating voltage for cell should be minimum [6]. The inverters are optimized for high noise margin[7] The use of SRAM is expected to increase in future for both portable and high performance microprocessor. SRAM plays a critical role in modern microprocessor system, portable devices like PDA, cellular phones, and portable multimedia devices [1]. To achieve higher speed microprocessor, SRAM based cache memories are commonly used. The trend of scaling of device brings several challenges like power dissipation, sub threshold leakage, reverse diode leakage, and stability [2]. Nowadays research on very low threshold voltage and ultra-thin gate oxide are in progressive stage, due to reduction in the threshold voltage and the gate oxide thickness. The phenomena like intrinsic parameter fluctuation, random dopant fluctuation, oxides thickness fluctuation, and line edge roughness further degrade the stability of SRAM cells [3-5]. Jaydeep P. Kulkarni [1]. The proposed shows ultra-voltage operation of different SRAM cell is explained The ultra-voltage operation is performed by lowering the supply voltage. The proposed ST-2-bit cell gives 1.6 times higher read static margin and 2 times write static margin as compare to 6T SRAM. For achieving low voltage operation 6T/8T/10T/ST SRAM topologies are studied in this paper. Results are carried out at 130nm technology, which give the effectiveness of proposed bit cell for successive ultra-low voltage operation. Mohsen Imani, Haleh Alimohamadi [2] proposed low power 12T SRAM cell with 16nm at 800mv supply voltage CMOS technology. The proposed 12T SRAM cell is compared with the 9T and 10T SRAM cell which shows that the leakage current is reduced by using two stack transistors at read path. The reliability of cell also increases by increasing read SNM. The proposed cell has 5.5% and 27.4% higher read SNM from 9T and 10T respectively. The power consumption of proposed 12T cell has lowered by 35.5% and 43.8% as comparison of 9T cell and 10T cell. Ambrish Mall, Suryabhan Pratap Singh, Manish Mishra, Geetika Shrivastava[3], states that this paper gives the brief development in low power circuit. In standby mode the power consumption is more. The proposed circuit contains a series connected tail transistor which turn down the leakage current which results in, low power consumption of cell. The proposed 12T SRAM cell is compared with low power 10T SRAM cell on 45nm and 32nm technology, it gives the power reduced by 45.94% (0.4v) and 31.08% (0.3v) respectively. K.G.Dharani [4], this paper gives the comparative analysis of 6T, 8T and 12T SRAM memory cell by power, layout and current values of the cell. In 6T, 8T, 12T the current values may be change during read and write operation but the power consumption is increased in 12T. But 12 T has a high capability to hold the data in the memory. This paper specifies that 6T has very less read margin with 8T transistor however 8T has high write noise margin. Mekala Tajeswar, P. Brundavani[5] ,in this paper, the operation of 12T SRAM cell on multi threshold CMOS technology are studied. This paper gives the reduction in power consumption of SRAM cell by adding transmission gate.By applying two sleep transistors the leakage current during hold mode is reduced and by applying two voltages at the output swing voltage is reduced. On the basis of power consumption, the proposed 12T SRAM cell is compared with the 6T SRAM cell, which shows that the power dissipation in 6T SRAM is 0.182mw and power dissipation at 12T SRAM is 0.169mw. Proposed clearly indicates 12T SRAM gives the better

performance and high speed data transmission with or without recovery boosting technique. M.Gangasukanya, P.Asiya Thapaswin[6], this paper introduced a 12T SRAM with high data transmission speed at 45nm technology and low power consumption. In this paper, proposed 12T SRAM cell is studied at different temperature.

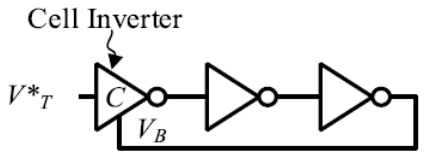
RANDOM-ACCESS MEMORIES (RAMS):

A random-access memory is a class of semiconductor memory in which the stored data can be accessed in any fashion and its access time is uniform regardless of the physical location. Random-access memories in general classified as read-only memory (ROM) and read/write memory. Read/write random-access memories are generally referred to as RAM. RAM can also be classified based on the storage mode of the memory: volatile and non-volatile memory. Volatile memory retains its data as long as power is supplied, while non-volatile memory will hold data indefinitely. RAM is referred as volatile memory, while ROM is referred as nonvolatile memory. Memory cells used in volatile memories can be further classified into static or dynamic structures. Static RAM (SRAM) cells use feedback (or cross coupled inverters) mechanism to maintain their state, while dynamic RAM (DRAM) cells use floating capacitor to hold charge as a data. The charged stored in the floating capacitor is leaky, so dynamic cells must be refreshed periodically to retain stored data. The positive feedback mechanism, between two cross coupled inverters in SRAM provides a stable data and facilitates high speed read and write operations. However, SRAMs are faster and it requires more area per bit than DRAMs.

STATIC RANDOM ACCESS MEMORIES:

Static Random Access Memories (SRAMs) continue to be critical components across a wide range of microelectronics applications from consumer wireless to high performance server processors, multimedia and System on Chip (SoC) applications. It is also projected that the percentage of embedded SRAM in SoC products will increase further from the current 84% to as high as 94% by the year 2014 according to the International Technology Roadmap for Semiconductors (ITRS). This trend has mainly grown due to ever increased demand of performance and higher memory bandwidth requirement to minimize the latency, therefore, larger L1, L2 and even L3 caches are being integrated on-die. Hence, it may not be an exaggeration to say that the SRAM is a good technology representative and a powerful workhorse for the realization of modern SoC applications and high performance processors. This chapter covers following SRAM aspects, basic operations of a standard 6-transistor (6T) SRAM cells and design metrics, nano-regime challenges and conflicting read-write requirements, recent trends in SRAM designs, process variation and Negative Bias Temperature Instability (NBTI), and SRAM cells for emerging devices such as Tunnel-FET (TFET) and Fin-FET. The basic operation of a SRAM cell as a storage element includes reading and writing data from/into the cell. Success of these operations is mainly gauged by two design metrics: Read Static Noise Margin (RSNM) and Write Static Noise Margin (WSNM). Apart from these metrics, an inline metric, N-curve is also used for measurement of read and write stability. The schematic diagrams and measurement process supported with HSPICE simulations results of different metrics will be presented in this chapter. As standard 6T SRAM cell has failed to deliver the adequate read and write noise margins below 600mv for 65nm technology nodes, several new SRAM designs have been proposed in the recent past to meet the nano-regime challenges. In standard 6T, both read and write operations are performed via same pass-gate transistors, therefore, poses a conflicting sizing requirement. The recent SRAM cell designs which comprise of 7 to 10 transistor resolved the conflicting requirement by providing separate read and write ports. SRAM cells are the first to suffer from the Process Variation (PV) induced side-effects. Because SRAM cells employ the minimum sized transistors to increase the device density into a die. PV significantly degrades the read and write noise margins and further exacerbates parametric yield when operating at low supply voltage. Furthermore, SRAM cells are particularly more susceptible to the NBTI effect because of their topologies.

ADAPTIVE BODY BIASING TECHNIQUE



(a)

Fig. (a) Conceptual diagram of the proposed adaptive body biasing circuit. (b) Simplified equivalent circuit of (a).

The variation in SNMs is a major issue in subthreshold memory design and it becomes more and more serious as the technology advances. Certain cell designs are more robust against variations [2]; yet, it is not clear how to generalize this counter-variation feature to other commonly used cells such as the read disturbfree 8T cell. To counteract threshold voltage

variations, one straightforward way is to increase the transistor sizing in a cell [8]. This way of remedy, however, introduces a large area penalty. Mismatches in transistors because of random dopant fluctuation are uncorrelated [9]. Therefore, compensation for local variation is not feasible. Global variation, however, can be sensed and compensated accordingly. To mitigate the threshold voltage variation, an adaptive body biasing technique is introduced in this section. A simple yet powerful body bias generation circuit is proposed, which senses global threshold voltage variations and then adjusts the body bias of SRAM cells for compensation. The circuit conceptually consists of only inverters, as shown in Fig.(a). To better understand how the proposed circuit functions, its simplified equivalent circuit is shown in Fig.(b). The first-stage sensing inverter senses and amplifies the difference between the desired transition voltage $V*T$ and the actual transition voltage VT. Two other inverters are employed as an error amplifier to further amplify the error. The error signal is then fed back to the cell inverter for a feedback control. The block T shown in the figure is the transfer function that models the relationship between the bias voltage of the cell inverter and the transition voltage of that inverter. In this paper, we use the body bias of PMOS transistors as an example, as this type of body biasing does not require any

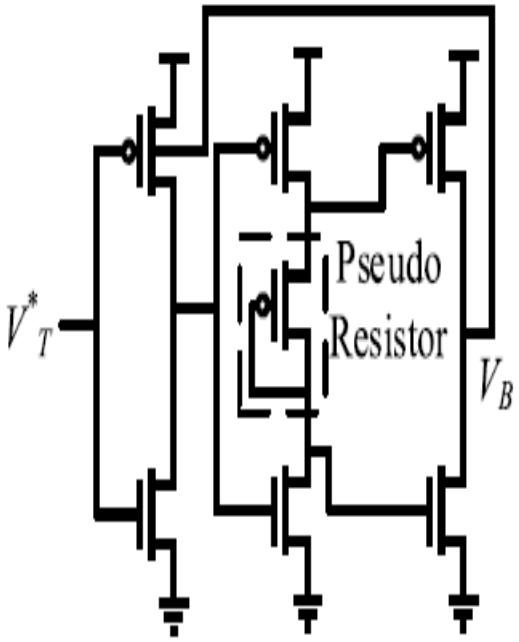


Fig. One example of generating body bias to mitigate the read SNM degradation when global variation is present. $V*T$ is the desired transition voltage.

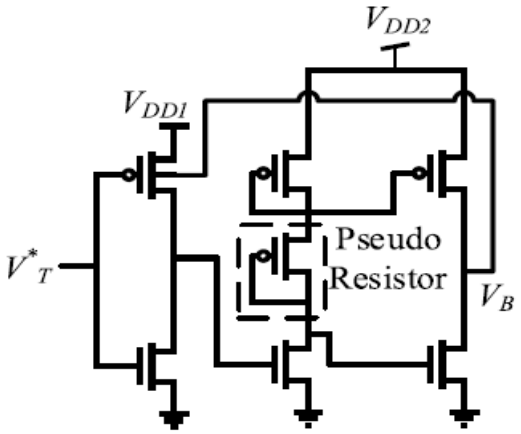


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Fig. Another example of generating body bias to mitigate read SNM degradation when the global variation is present. In the figure, $VDD2 > VDD1$. Compared to the circuit in Fig., the tuning range of the body bias is extended.

special option such as the triple-well process. Nevertheless, the proposed technique can be readily applied to the body biasing of NMOS transistors. Two examples of the proposed biasing circuit are shown in Fig. The circuit shown in Fig. requires an additional supply voltage so that the tuning range of the body bias can be enlarged. Despite its simplicity, one thing that needs to be ensured for the proposed adaptive biasing circuit is the stability. Inspired by the stabilization technique employed in a ring amplifier [3], an offset is introduced by the pseudo-resistor in Fig. In order for the two transistors at the output stage to conduct a small amount of current in the steady state. Therefore, a dominant pole is formed at the output stage, stabilizing the feedback circuit. In addition, the output of the biasing circuit is connected to bodies of many transistors in an SRAM array. The parasitic capacitance and body leakage current also help stabilize the loop

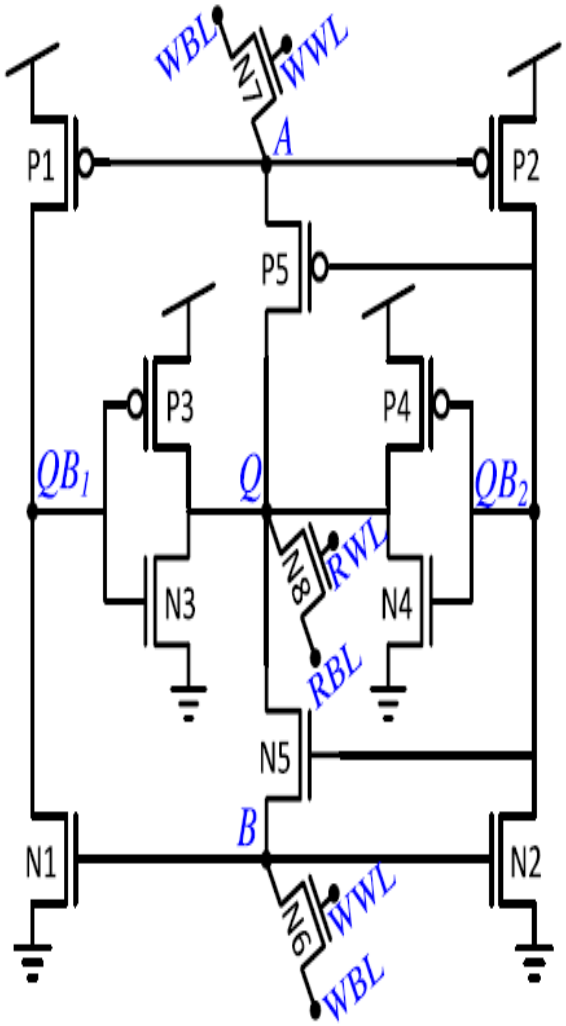
PROPOSED TECHNIQUE:

13T RADIATION TOLERANT BITCELL:

Bitcell Design

SRAM design for low-voltage operation has become increasingly popular in the recent past. Various bitcell designs and architectural techniques have been proposed to enable operation deep into the subthreshold region [15], [18]–[21]. These designs generally incorporate the addition of a number of transistors into the bitcell topology, compared with the baseline 6T SRAM bitcell, trading off density with robust, low-voltage functionality. However, these bitcells were designed for operation under standard

operating environments, and thereby, do not provide sufficient robustness to SEUs under high-radiation conditions. In addition, the design architecture of these cells is based on the standard 6T cell; therefore, the 6T cell has the same hardening ability to most, if not all, these unprotected cells.



The proposed 13T bitcell features two stable states, representing a logic 1 and a logic 0, defined as the voltage level at node *Q*. The ON/OFF states of the devices and the resulting voltage state at the internal nodes are shown in Fig. . Similar to a standard cross-coupled inverter structure, inverted voltage levels are held at the internal data nodes. Starting with the logic 1 state [Fig. 3(a)], the low level at *QB*2 enables *Q* to charge *A* to *V*DD through P5, thereby cutting off P1 and P2 and eliminating any pull-up currents to *QB*1 and *QB*2. Leakage currents from the strongly driven *Q* node through N5 charge node *B*, thereby turning ON N1 and N2 and enabling a

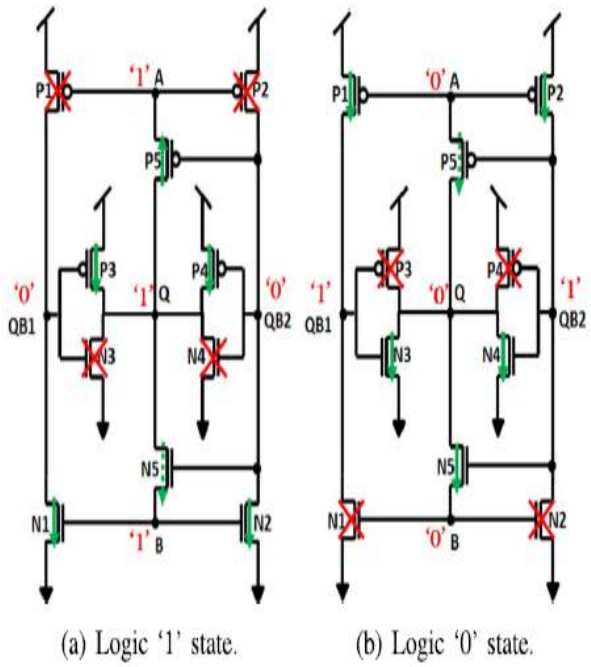


Fig. Stable states of the 13T bitcell. For simplicity, devices N6–N8 were omitted from this figure.

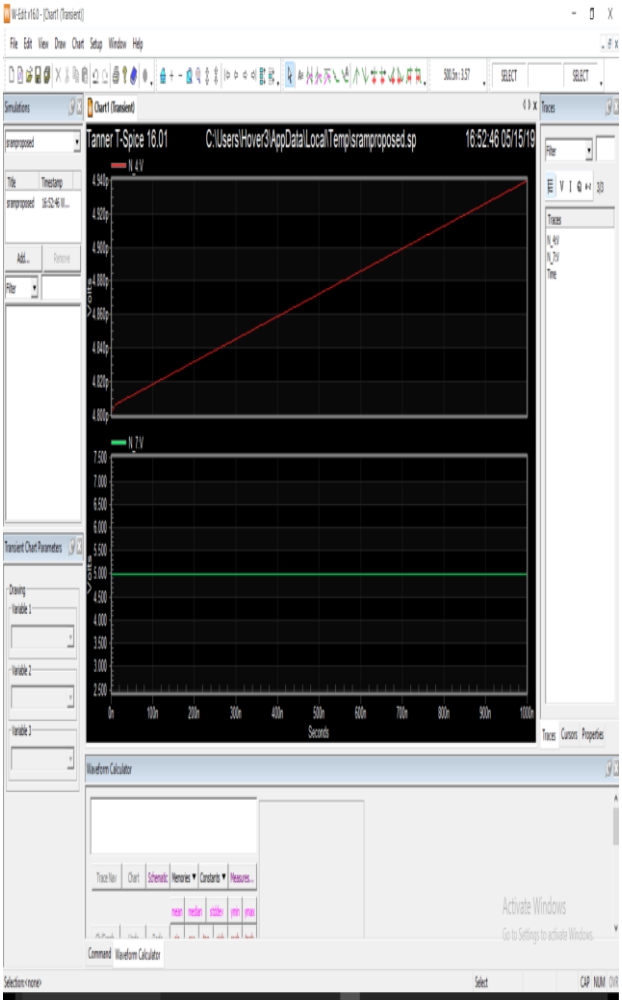
discharge path to assist in holding *QB*1 and *QB*2 at 0. Note that both nodes *A* and *B* are driven to a predetermined level during the write operation, as described below, and therefore are not reliant on the aforementioned leakage currents to set the initial storage level of the cell. An almost symmetric process occurs in the logic 0 state, as shown in above figure. In this case, *QB*2 is high, allowing *B* to discharge through N5 to *Q* and cutoff the pull-down paths from *QB*1 and *QB*2 through N1 and N2, respectively. Any charge stored at node *A* will leak through P5 to *Q*, enabling pull-up paths through P1 and P2 to *QB*1 and *QB*2 in order to replenish any charge lost at these nodes.

INHERENT SEU TOLERANCE

Two basic principles provide the proposed bitcell with inherent SEU tolerance. 1) The data are read out from node *Q*, such that any temporary upset on other nodes can be tolerated. 2) The assisting nodes are designed with redundancy to ensure that any upset will be mitigated by the other nodes. When a radiation strike causes a value change on any node of the bitcell, the other four internal nodes are designed, so that the state change at this node cannot flip the cell and the disruption is suppressed within a deterministic recovery time. For example, an upset at *Q* will quickly be suppressed through the dual-driven mechanism created by the internal inverters. Due to their

separated nature, upsets at *QB*1 and *QB*2 will not be able to change the state at *Q* and will return to their original state.

RESULT:



CONCLUSION*:*

This paper proposes a 13T SRAM memory bitcell which is robust, low-voltage, ultra-low Power operations in the highly-radiated environments. The mechanism proposed is novel dual-driven separated mechanism which has high tolerance for the soft errors and robust to low supply voltage. Single event upset probability is decreased while the bitcell area is maintained to be much smaller than the alternative solutions like TMR which will result in only two times larger area than conventional 6T approach. A decoder is added for the memory array and a sense amplifier is used for the read circuitry where it senses low power signals from a bit line and represents a data bit (0 or 1) stored in a memory and amplifies the voltage swing to recognizable logic level. Tristate buffer is added to control the data.

FUTURE ENHANCEMENT:

On the basis of the studies and the investigations carried out in this research, as an extension of this work the following points are suggested. x The 8T and 10T SRAM cell can be implemented with 120 nm, 90 nm and 32 nm CMOS technology for the above low power techniques. x 12T SRAM cell can be implemented with 120 nm,90 nm and 32 nm CMOS technology for the same logic. x Temperature analysis can also be done for all the circuits using hotspot tool. x Static Noise Margin(SNM) is one of the parameters for designing any SRAM circuit. So, this can be considered for 8T,10T and 12T SRAM cell with 4x4 SRAMs cell array. x To increase the pull-up ratio, the speed of operations of SRAM cell increases. Further, to increase the performance of SRAM cell, the SNM and pull-up ratio can be varied for the design of SRAM cell. x This designed circuit can be implemented with any type of processor recently used in markets.

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